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# **ADVANCED IC PACKAGING TECHNOLOGIES, MATERIALS, AND MARKETS**

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**2011 EDITION**



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# CHAPTER 1

## INTRODUCTION

### 1.1 BACKGROUND

The demand for mobile electronics that keep us connected all the time spiked the demand for integrated circuits (ICs) in 2010 to record levels. The year 2010 saw growth of 31.3 percent in revenue and 28.9 percent in units over 2009. The IC industry saw demand rise faster than did most other industries.

In 2011, there are:

- 1 billion transistors for every human
- 100 billion “smart devices”
- 10 billion devices connected to the Internet<sup>1</sup>
- Worldwide mobile connections of 5.6 billion, up 11 percent from 5 billion connections in 2010<sup>2</sup>

The demand for digital devices and Internet services is expected to bring the following increases by 2015:

- 1 billion more Internet users
- 10 billion more connected devices
- 8 times more Internet traffic and 16 times more storage<sup>3</sup>

The demand for mobile electronic devices is increasing, whereas the time in which the first 10 million units sold is decreasing. Some examples of this are:<sup>3</sup>

- 2007      iPhone            17 months
- 2008      Netbook            15 months
- 2010      iPad                8 months
- 2011      Xbox Kinect      4.5 months

What this is pointing to is an opportunity to innovate, with the ability to win back the initial investment in a fairly short time period if the product is well received on the market. Shorter product life spans are another possibility, if new innovations take the space of recently introduced products.

## 1.2 SCOPE

This report covers these basic topics:

- Stacked packages
- Through-silicon vias (TSVs), including 3-D and 2.5-D
- System in package (SiP)
- Fan-in QFN packages
- WLPs, including fan-out WLPs
- Interconnection, flip chip, bumping, wire bonding, and wire bond material
- Substrates
- Consumer mobile applications

## 1.3 ORGANIZATION

This report is divided into ten chapters and two appendices. They are as follows:

**Chapter 1, Introduction:** This chapter outlines the background, scope, organization, and methodology of the report.

**Chapter 2, Executive Summary:** This chapter provides summary forecasts and information.

**Chapter 3, Stacked Packages:** Stacked packages are covered, including discussions of the stacking technology and wafer thinning that enable this technology, applications, new product highlights, and forecasts of the technology. Forecasts of the different stacked package types include units, package

assembly pricing, and packaging revenue, by stacked package style. The different stacked packaging styles include die stacks, PoP, or package stacks, PiP, TSOP stacks, QFN stacks, MCM stacks, and WLP stacks. These packages are also presented as a percentage of the total market for the package type in which they belong. Stacked package forecasts also include device types (memory, logic, etc.), interconnection (wire bonding, flip chip, through-silicon vias), and applications.

**Chapter 4, Through-Silicon Vias or 3-D Integration:** Both 3-D and 2.5-D integration are covered in this chapter. Discussions include die-to-die, die-to-wafer, and wafer-to-wafer bonding; via first, middle, and last; etching and filling; specific upcoming applications, new product/technology highlights, and discussions. Forecasts include 2.5-D, 3-D, and the market potential for this technology.

**Chapter 5, System in Package:** Coverage of SiPs in this chapter includes discussions of technology trends, new product introductions, and forecasts. Forecasts include units, package assembly pricing, packaging revenue, device types (memory, logic, etc.), interconnection (wire bonding, flip chip, etc.), and applications.

**Chapter 6, Fan-In QFN Packages:** An overview of these leadframe-based packages is followed by new product introductions. Market forecasts include units, average I/O count, price per I/O, average assembly price, and revenue.

**Chapter 7, Wafer-Level Packages, Including Fan-Out WLPs:** This chapter begins with a discussion of WLP technology. The distinction between WLPs and wafer bumping for flip chip devices is explained. New product introductions of WLPs are then presented. A forecast of WLPs by markets, major product category, I/O pitch, and fan-out WLPs is included.

**Chapter 8, Interconnection, Flip Chip, Bumping, and Wire Bonds:** This chapter reviews the basics of first-level interconnection and bumping and discusses new product introductions. Forecasts of interconnection for QFN,

DFN, PGA, BGA, and FBGA packages are presented, for both wire bond and flip chip units. Total wire bonded package units are forecast, as is the total wire bond usage by material type and wire width.

Flip chip units are forecast both in-package and as direct chip attach (DCA). Bumping costs are also divulged. Further forecasts delve deeper into the bumping process, and include the UBM process and bump. Flip chip in package assembly prices and revenue are provided.

The chapter concludes with a complete interconnection forecast of in-package, on-the-board, and wafer-level packages.

**Chapter 9, Substrates:** A review of substrate options is followed by forecasts by pitch for PGA, BGA, and FBGA, and by substrate units, substrate area, and substrate revenue for various substrate types organized by PGA, BGA, and FBGA packages.

**Chapter 10, State of the Industry and Applications for IC Devices:** This chapter contains an overview of current market status, and covers mobile electronic applications for IC devices by product group, the total number of ICs for each product category, and total IC revenue.

**Appendix A, Website Address Guide:** This appendix contains the Internet addresses of the companies presented in this report.

**Appendix B, Glossary:** This appendix contains a general glossary of terms used in the IC packaging industry.

## 1.4 METHODOLOGY

Information was obtained from both primary and secondary sources to complete this report. Information was gathered by telephone, facsimile, and e-mail, at trade shows, from speakers at seminars, conferences, luncheons, and dinners, and by visiting companies in the industry. Secondary sources of information included company literature, trade magazines, seminar proceedings, and the Internet, and often led to further primary contact.

Hundreds of individuals were contacted for information for this report. They included key people within all of the major semiconductor fabrication companies and IC package foundries around the globe. Information was obtained using standard surveys and is printed only in the aggregate. The survey questions were designed to determine the size of the market and likely growth patterns and to elicit responses about issues and developments in this particular area of the packaging industry. Discussions with those in the industry also played a key part in gathering information for this report.

A wide assortment of companies providing products and services for this market was contacted as well. Information was gathered in person when possible; company literature and white papers from seminars and proceedings were also heavily utilized.

### **Chapter Notes**

1. Walker, Jim, Gartner. “More with Less: The Challenging Dynamics of Semiconductor Packaging.” Presented at SEMICON West, TechXPOT North Two, July 13, 2011.
2. Gartner Newsroom. “Gartner Says Worldwide Mobile Connections Will Reach 5.6 Billion in 2011 as Mobile Data Services Revenue Totals \$314.7 Billion.” August 5, 2011.
3. Greyeli, Nasser, Ph.D., Intel Corporate Quality Network. “Challenges and Opportunities Ahead...Are We Ready for the Future of the Digital World?” ECTC Luncheon, Lake Buena Vista, Florida, June 1, 2011.