
IC PACKAGE PITCH, LEADFRAME PLATING, AND SUBSTRATE MARKETS

2013 EDITION

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The backbone of each report is based upon primary market research information. Our market information originates from direct interviews with vendors, users, and other industry participants. We use secondary research to test for reasonableness, technical backgrounds, and, in some cases, for top-level forecasts. We distill the research into coherent forecasts and recommendations.

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Chapter 1

INTRODUCTION

1.1 Background

IC packaging has taken a prominent role in enabling the advancement of mobile computing and meeting the requirements of high bandwidth. Because IC packaging holds the footprint to the printed circuit board (PCB), the size of the package is a large factor in the size of today's electronic gadgets. With Moore's Law nearly reaching its physical limitations, it is the ability to shorten the electrical signal path of the packaging of the integrated circuit (IC) that in turn enables faster signal propagation, thus allowing for meeting the higher bandwidth requirements.

Reducing the pitch of the package is one method of reducing the package size and shortening the electrical path. This report contains information on pitch, substrates, and plating finish, and is a continuation of the full coverage on the topic of IC packaging in this year's IC packaging series.

1.2 Scope

This report covers these basic topics:

- IC package pitch
- Leadframe finish
- IC package substrates for array packages

1.3 Organization

This report is divided into six chapters and two appendices. They are as follows:

Chapter 1, Introduction: This chapter outlines the background, scope, organization, and methodology of the report.

Chapter 2, Executive Summary: This chapter provides summary forecasts and information.

Chapter 3, Economic Outlook and Worldwide Electronics Industry Forecast, is an overview of the state of the overall economy and semiconductor industry.

Chapter 4, IC Package Pitch by Major Package Family and I/O Count Range.

The major package families include:

- Dual in-line package (DIP)
- Small outline transistor (SOT)
- Small outline (SO)
- Thin small outline package (TSOP)
- Dual flat pack no lead (DFN)
- Chip carrier (CC)
- Quad flat pack (QFP)
- Quad flat pack no lead (QFN)
- Pin grid array (PGA)
- Ball grid array (BGA)
- Fine-pitched ball grid array (FBGA)
- Wafer-level package (WLP)

The pitch forecasts are given for the I/O ranges of 3–18, 20–32, 34–100, 102–304, 308–999, and 1,000 and up. The global figures for the package families come from NVR's *The Worldwide IC Packaging Market, 2013 Edition*, the first report in this four-report series of 2013. Those figures are built up from the package options of all IC device types, such as MPU, DRAM, the various analog chips, etc.

Chapter 5, Leadframe Plating Options and Lead-Free Issues, presents the forecasts for the leadframe plating options of the major leadframe package families of DIP, SO, SOT, TSOP, DFN, QFP, and QFN, and discusses the issues and solutions surrounding lead-free electronics.

Chapter 6, Substrates, forecasts the substrate options for the major packaging families of PGA, BGA, and FBGA. Forecasts of the various substrate options are presented by package family, substrate units, substrate area, and substrate revenue.

Appendix A, Website Address Guide: This appendix contains the Internet addresses of the companies presented in this report, plus the OSAT companies that serve the IC packaging industry.

Appendix B, Glossary: This appendix contains a general glossary of terms used in the IC packaging industry.

1.4 Methodology

Information was obtained from both primary and secondary sources to complete this report. Information was gathered by telephone, e-mail, at trade shows, from speakers at seminars, conferences, luncheons, and dinners, and by visiting companies in the industry. Secondary sources of information included company literature, trade magazines, seminar proceedings, and the Internet, and often led to further primary contact.

Hundreds of individuals were contacted for information for this report. They included key people within all of the major semiconductor fabrication companies and IC package foundries around the globe. Information was obtained using standard surveys and is printed only in the aggregate. The survey questions were designed to determine the size of the market and likely growth patterns and to elicit responses about issues and developments in this particular area of the packaging industry. Discussions with those in the industry also played a key part in gathering information for this report.

A wide assortment of companies providing products and services for this market was contacted as well. Information was gathered in person when possible; company literature and white papers from seminars and proceedings were also heavily utilized.