ADVANCED IC PACKAGING TECHNOLOGIES, MATERIALS, AND MARKETS

2015 EDITION

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Chapter 1
Introduction

1.1 Scope of the Report

Moore's Law—the assertion originally posited by Gordon E. Moore, co-founder of Intel Corp., that the number of transistors packed into an integrated circuit will double every two years (now considered to be every 18 months)—has effectively defined the expansion of the electronics industry for nearly half a century. However, there is strong evidence that this particular "law" is about to be broken, that the pace of the integration of transistors must soon begin to slow, if it has not already done so. On the other side are the optimists who insist that new materials and technologies will continue to drive the industry to ever-greater densities and levels of complexity.

The demand for consumer electronics and mobile communications devices that keep us connected is driving electronics manufacturers to deliver ever-more compact and portable electronics. Today's users ask for electronics with more functionality, added performance, higher speed, and smaller form factors. With the push toward higher densities, though, the cost per transistor is gradually going up. Consequently, over the past decade or so, the original concept of Moore's Law has been augmented by a new concept known as More than Moore, which incorporates the "added value" provided to devices by other technologies that do not necessarily scale according to Moore's Law.

More than Moore includes (among other things) the realm of advanced IC packaging, the techniques and technologies that make it possible to assemble ICs in ever more dense packages. This is where semiconductor packaging becomes more than a means of protecting the delicate ICs and enabling an efficient way of connecting them to the other components of the products they make possible. So, rather than depend only on the increasing integration of the monolithic devices at the front end of the semiconductor manufacturing process, manufacturers are relying more and more on the back end, and on configurations that enable multiple monolithic ICs to be interconnected in smaller and smaller packages.

This report provides an analysis of and forecasts for advanced IC packaging technologies and materials. It is to some extent an extension of New Venture Research's *The Worldwide IC Packaging Market, 2014 Edition*, published in mid-2014. However, rather than provide a broad overview of the entire IC packaging market, this report focuses, instead, on the most advanced types of IC packages being developed and shipped today: so-called multichip packages (MCPs) as well as unique single-chip solutions. We are, in essence, taking a subset of the overall IC packaging market and concentrating on the leading-edge products. Specifically, this report looks at these market segments:

- Stacked IC packages: packages that combine multiple die of a given type—e.g., thin small outline packages (TSOPs), fine-pitch ball grid arrays (FBGAs), and wafer level packages (WLPs)—usually in vertical stacks that are then packaged as a single chip
- System-in-package solutions: packages that combine not just stacks of one type of device, but a variety of devices, including passive components. Examples of these advanced packages are package in packages (PiPs), package on packages (PoPs), and multichip modules (MCMs)
- Advanced forms of single-chip devices, specifically fan-out wafer-level packages (FOWLPs) and multi-row quad flat pack no lead packages (QFNs)
- Advanced interconnection technologies, specifically flip chip and through-silicon vias (TSVs), with a discussion of current trends in traditional wire bonding techniques
- Substrate materials and technologies that augment the advances achieved with multichip packages

Each market segment covered in this report includes an overview of the technology and general market trends, plus quantitative analyses with forecasts of unit shipments, revenues, pricing, etc. Data in tables cover the historical years 2013 and 2014, with forecasts provided through 2019. In addition, we provide a close look at the activities of selected competitors in the advanced IC packaging marketplace.

1.2 Report Organization

1.2.1 Methodology

The information presented in this report was gathered from a variety of primary and secondary sources. The primary sources were engineering, marketing, and business development managers at IC packaging manufacturers, fabless companies, and foundries and IDMs, who were contacted directly. These individuals were asked to respond to a written survey. In addition, extensive use was made of secondary source materials, including company Web sites and literature, such as press releases and investment reports; articles and white papers obtained through online databases and trade publications; and of course extensive use of resources on the open Internet. New Venture Research and the author are the sole and exclusive developers of the data used in forecasts that appear in this report.

1.2.2 Chapter Outline

This report is organized into eight chapters, plus a Glossary:

- Chapter 1. Introduction – Outlines the scope and organization of the report.
- Chapter 2. Executive Summary – Provides an overview of the market and highlights of the top-level market segments.
- Chapter 3. Review of the Worldwide IC Packaging Marketplace – Provides a brief review of the broader IC packaging marketplace more fully detailed in the companion report, *The Worldwide IC Packaging Market, 2014 Edition*. This chapter also analyzes the application trends for IC packaging markets.
- Chapter 4. Interconnection Techniques – Describes the market and technology trends of wire bonding, the dominant type of interconnection for all packaging technologies, as well as advanced methods of interconnection, including flip chip and through-silicon vias. Forecasts of market segments are provided.
- Chapter 5. Multichip Packages – Describes the market and technology trends of packages comprised of two or more die, including stacked

TSOPs, stacked BGA/FBGAs, stacked QFNs, package on packages (PoPs), package in packages (PiPs), multichip modules, and stacked wafer-level packages. Forecasts of market segments are provided.

- Chapter 6. System-in-Package Solutions and Substrate Materials – Analyzes multicomponent packages that provide a functional unit in a single package. This market segment is comprised of PoPs, PiPs, MCMs, and a subset of stacked WLPs. Also discusses advances in substrate material technology used with SiPs.
- Chapter 7. Advanced Single-Chip Packages – Describes the market and technology trends of somewhat exotic advanced packages that do not necessarily involve multiple die. Specific packages include multi-row QFNs and fan-out WLPs. Forecasts of market segments are provided.
- Chapter 8. Advanced IC Packaging Company Profiles – In-depth profiles of industry participants.
- Glossary

1.3 Terminology Conventions

One of the idiosyncrasies of the universe of high-tech electronics is its tendency to twist terminology to fit a technology or concept (e.g., this report is about the semiconductor "space"), or even to invent new words when it suits (Shakespeare did the same thing and look at what it did for him). This unique terminology and alternate spellings of words tend to be proliferated throughout the industry and the media. For example, the dictionary term *three-dimensional* is "traditionally" abbreviated as 3-D, owing to the hyphen in the spelled-out term. However, in trade press articles and on the Internet, we see the abbreviation variously as *3-D, 3D,* or *3 D.*

For purposes of this report, we will standardize on spelling this and other terms, as they are commonly used (or perceived to be commonly used) within the semiconductor industry. Therefore, throughout this report we use the following conventions for spelling of common technical and not-so-technical terms:

- 3D – Three-dimensional
- 2D and 2.5D – Two-dimensional and two-point-five-dimensional

- Flip chip (no hyphen, two words)
- Packaging types such as BGA and WLP are all caps, as acronyms, but when spelled out, no capitalization is used; thus, ball grid array and wafer-level packaging. However, initial caps may be used when introducing the term for the first time.
- Multichip packaging, multichip modules, multicomponent ICs, etc. (no hyphen, one word), but "single-chip" ICs because this is not a commonly accepted term of the semiconductor space, per se. (See, even we fall prey to the new jargon!)

Where a specific product name of a particular company differs from our conventions, especially in the case of trademarked and registered names, the formal name takes precedence—for example, Siliconware's "Multi-Package BGA" or the company "FlipChip International." The Glossary provides the spelling of many words and phrases that appear throughout this report.

Finally, we should point out that there are few direct quotes to be found in this report, although we have utilized many sources, both traditional publications and those "published" on the Internet, as well as direct contacts with industry participants. Care has been taken that the text used throughout this report is our own. However, where the resource is in the public domain—such as Web-based marketing material or text and images placed on the Internet and intended for public consumption—a limited amount of verbatim text may be used. To be specific, managers may recognize in their company profiles some descriptive materials as it pertains to their own company and products. In no way, however, do we intentionally plagiarize or make public proprietary information that has been provided in confidence to NVR or the author of this report.

Having said this, relevant to the conventional use of grammar, we include the following quote from Clive "Max" Maxfield's excellent overview of electronics, *Bebop to the Boolean Boogie*: "Except where such interpretation is inconsistent with the context, the singular shall be deemed to include the plural, the masculine shall be deemed to include the feminine, and the spelling (and the punctuation) shall be deemed to be correct!"