# ADVANCED IC PACKAGING TECHNOLOGIES, MATERIALS, AND MARKETS

## 2016 EDITION


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New Venture Research (NVR) was formed in 1988 to assist industry executives in their decision making. We began as an independent consultancy and have recently evolved into a publisher of off-the-shelf market research reports in key areas of the electronics industry. The reports are written by a team of staff analysts and independent consultants. We also offer consulting services when our clients need information not found in our reports.

The backbone of each report is based upon primary market research information. Our market information originates from direct interviews with vendors, users, and other industry participants. We use secondary research to test for reasonableness, technical backgrounds, and, in some cases, for top-level forecasts. We distill the research into coherent forecasts and recommendations.

We are dedicated to providing our customers with accurate reporting on our targeted markets. One of our reports can save our customers months or years of research. The reports enable executives to make decisions in a structured manner. Our customers tell us these reports are excellent tools for building consensus regarding their company's real market opportunities.


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# Advanced IC Packaging Technologies, Materials, and Markets, 2016 Edition

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# Chapter 1
# Introduction

## 1.1 Objectives of the Report

This 2016 edition of *Advanced IC Packaging Technologies, Materials, and Markets* report provides a detailed analysis and forecasts for a particular segment of the global market for integrated circuits (ICs) packaging. It is closely related to and gets much of its underlying data from New Venture Research's *Worldwide IC Packaging Markets, 2015 Edition*. However, rather than provide a broad overview of the entire IC packaging market, this report focuses, instead, on the most advanced types of IC packages being developed and shipped today—advanced versions of otherwise standard chip packages, as well as a range of so-called multichip packages (MCPs)—and on new techniques and materials used in manufacturing these advanced IC packaging solutions. The report, in essence, concentrates on a subset of the overall IC packaging market: the leading-edge products and technologies of the IC packaging industry.

This report is designed to aid executives and management within sales, business development, and marketing organizations in making important strategic and product development decisions. Toward that aim, it provides qualitative analysis of the covered market segments, as well as current statistical data and forecasts that will enable companies and individuals to better understand the status of the market, as well as anticipate market trends.

## 1.2 Scope of the Report

The manufacturing of semiconductors is an extremely complex and capital-intensive process. In its most simplified form, the manufacturing process requires five major steps: circuit design, wafer fabrication, wafer test, assembly and packaging (the words are sometimes used synonymously), and final test. The first three steps are collectively known as the "front end" and involve the design and production of the semiconductor devices; the fourth and fifth steps are the "back end" and often referred to as simply "assembly and test."

This report focuses on the assembly or IC packaging step of the process, and the companies that provide IC packaging products and solutions. Further, the subjects of this report are the most advanced forms of IC packaging solutions being delivered today. Specifically, the market segments covered in this report are:

- Fan-out wafer-level packages (FOWLPs) and multi-row quad flat pack no lead (QFN) packages—these are recent advancements aimed at expanding the number of leads or connections beyond the numbers the standard chips are capable of.
- Stacked IC packages—packages that combine multiple die of a given type in vertical stacks that are then packaged as a single chip. Specific market segments that are analyzed include thin small outline packages (TSOPs), fine-pitch ball grid arrays (FBGAs), QFNs, and wafer-level packages (WLPs).
- System-in-package solutions—these packages combine not just stacks of one type of device, but a variety of devices, including logic, memory, and passive components. Examples of these advanced packages are package in packages (PiPs), package on packages (PoPs), and multichip modules (MCMs).
- Advanced interconnection technologies, specifically flip chip and through-silicon vias (TSVs). The section also includes a discussion of current trends in traditional wire bonding techniques.
- Substrate materials and technologies that augment the advances achieved with multichip packages.

Each market segment covered in this report includes an overview of the technology and general market trends, plus quantitative analyses with forecasts of unit shipments, revenues, pricing, etc. Data in tables cover the historical years 2014 and 2015, with forecasts provided through 2020.

In addition, we provide individual profiles of selected competitors in the advanced IC packaging marketplace. The field of manufacturers who provide IC packaging solutions is quite large and varied. The largest and (mostly) oldest semiconductor companies—IBM, Intel, Fujitsu, Mitsubishi, NEC, NXP (formerly a division of Philips), and Samsung, to name a few—have the internal resources to carry out both front- and back-end processes in the semiconductor manufacturing process. These have come to be known as integrated device manufacturers (IDMs). However, numerous other companies have risen over the years that specialize solely in the back-end processes. These are collectively known as outsourced semiconductor assembly and test (OSAT) companies, and it is from this group that we selected companies with specific advanced IC packaging product lines to profile.

## 1.3 Report Organization

### 1.3.1 Grammatical Conventions

Perhaps more than most, the electronics sector tends to use terminology in a unique and sometimes confusing way. Abbreviations or acronyms for both technical and nontechnical terms are very common—but not very consistent. For example, the standard dictionary method of abbreviating the term *three-dimensional* is "3-D." However, in trade press articles and on the Internet and even in scientific papers, we see the abbreviation variously as *3-D, 3D,* or *3 D*. Similar variations are true for many common semiconductor and packaging terms.

For purposes of this report, we use the following conventions for spelling of common technical and not-so-technical terms:

- 2D, 2.5D, and 3D to abbreviate the types of packaging discussed throughout the discussion of multichip packaging
- Flip chip (no hyphen, two words)
- Multichip packaging, multichip modules, multicomponent ICs, etc. (no hyphen, one word), but single-chip packaging and multi-row QFN.
- Packaging types such as FBGA and WLP are all caps as acronyms, but when spelled out, no capitalization is used; thus, fine-pitch ball grid array and wafer-level package.
- Other acronyms may vary as to capitalization. In particular, terms that include prepositions, such as system-in-package (with hyphens), package in package and package on package (no hyphens) are rendered as SiP, PiP, and PoP, respectively. Internet of Things (note the caps) is abbreviated as IoT. Similarly, the term "year-over-year," which appears in tables throughout the report, is abbreviated "YoY."

Where a specific product or brand names differ from our conventions, especially in the case of trademarked and registered names, the formal name takes precedence—for example, Siliconware's "Multi-Package BGA" or the company "FlipChip International." The Glossary provides the spelling of words and phrases that appear throughout this report.

Finally, we should point out that there are few direct quotes to be found in this report, although we have consulted many sources, including traditional publications and Internet-only sources (blogs, e-zines, etc.), as well as direct contacts with industry participants. Care has been taken that the text used throughout this report is our own. However, where the resource is in

the public domain—such as Web-based marketing material or text and images placed on the Internet and intended for public consumption—a limited amount of verbatim text may be used. To be specific, managers may recognize in their company profiles some descriptive materials as it pertains to their own company and products. In no way, however, do we intentionally plagiarize or make public proprietary information that has been provided in confidence to NVR or the author of this report.

### 1.3.2 Methodology

The information presented in this report was gathered from a variety of primary and secondary sources. Both qualitative and quantitative data were provided by marketing and business development managers at IC packaging manufacturers and other semiconductor-related companies through responses to detailed surveys. In addition, extensive use was made of publicly available materials, including company Web sites and literature such as press releases and investment reports, as well as articles and white papers obtained through the Internet, online databases, and trade publications. We have utilized these varied resources to ascertain market trends and in preparing the tables and figures appearing throughout this report. However, the author and New Venture Research are the sole and exclusive originators of the specific historical and forecast data presented in this report, and are responsible for its content.

### 1.3.3 Chapter Outline

This report is organized into eight chapters, plus a Glossary:

- Chapter 1 Introduction—Outlines the scope and organization of the report.
- Chapter 2 Executive Summary—Provides an overview of the market and highlights of the top-level market segments.
- Chapter 3 Overview of Worldwide IC Packaging Markets—Provides a brief review of the broader IC packaging marketplace more fully detailed in the companion report, *TheWorldwide IC Packaging Market, 2015 Edition*. This chapter also analyzes the application trends for IC packaging markets.
- Chapter 4 Advanced Single-Chip IC Packaging—Describes the market and technology trends of somewhat exotic advanced packages that do not necessarily involve multiple die. Specific packages include multi-row QFNs and fan-out WLPs. Forecasts of market segments are provided.

- Chapter 5 Multichip Packaging Markets—Describes the market and technology trends of packages comprised of two or more die, including stacked TSOPs, stacked BGA/FBGAs, stacked QFNs, package on packages (PoPs), package in packages (PiPs), multichip modules, and stacked wafer-level packages. Forecasts of market segments are provided.
- Chapter 6 System-in-Package Solutions and Substrate Materials—Analyzes multicomponent packages that make up a functional unit (i.e., a complete system) in a single package. This market segment is comprised of PoPs, PiPs, MCMs, and a subset of stacked WLPs. Also discusses advances in substrate material technology used with SiPs.
- Chapter 7 Interconnection Technologies and Solutions—Describes the market and technology trends of wire bonding, the dominant type of interconnection for all packaging technologies, as well as advanced methods of interconnection, including flip chip and through-silicon vias (TSVs). Forecasts of market segments are provided.
- Chapter 8 Advanced IC Packaging Company Profiles—In-depth profiles of industry participants.
- Glossary