Global IC Packaging Applications and Outsourced Semiconductor and Test (OSAT) Markets

2019 EDITION

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ABOUT THE AUTHOR

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Chapter 1
Introduction

1.1 Report Overview

This report, *Global IC Packaging Applications and Outsourced Semiconductor and Test (OSAT) Markets, 2019 Edition,* provides a comprehensive examination of integrated circuits with a specific focus on the applications for which ICs are made. We start with an examination of the global electronics market with respect to IC devices used in electronics products. The report then provides an overview of worldwide markets for IC devices and IC packaging, as a preliminary to understanding the applications for which ICs are produced. The comprehensive analysis of applications includes discussions of the IC device functions (processors, logic, memory, and analog) as well as individual IC packaging market segments. Supporting our extensive qualitative analysis are numerous tables and figures providing 2018 market data and five-year forecasts through 2023. In most cases we provide data for both annual unit shipments and revenues for each market segment and application segment covered in the report.

In its final chapters, this report continues NVR's long-standing coverage of the OSAT market—vendors that specialize in providing IC packaging and testing services to other companies in the industry. Consisting of more than 200 companies worldwide, the OSAT market segment accounts for a significant and growing sector of the semiconductor market. The report looks not only at the size of the OSAT market, but discusses the various strategies for success shared by the leading competitors. Finally, the report includes company profiles of 39 OSAT companies, providing a cross-section of both large and small competitors. Each profile includes an overview of the company, as well as details of its IC packaging product lines.

The data underlying the quantitative analysis and qualitative discussions in this report was gathered from a variety of primary and secondary resources. NVR contacted individual business and marketing managers at semiconductor companies to invite participation in our industry survey consisting of a series of questions related to their IC packaging products and the applications for which they are made. The primary goal of the questions we asked was to understand the current status of the demand for products and the direction in which the industry is heading. More specific data related to individual companies was obtained through press releases, investment reports (e.g., annual reports and SEC filings), white papers, etc. Other resources we consulted included online databases, trade publications, and a wide variety of publications available on related industry Web sites.

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To ground our findings in reality, we relied on our own previous reports, as well as historical industry data obtained from other sources, including the SIA's World Semiconductor Trade Statistics (WSTS) database. Based on the survey responses we received and other information we compiled, we have determined the major trends driving the market and developed a framework for forecasting the future direction the market is likely to take.

This report provides information critical for companies involved in semiconductor manufacturing and IC assembly and test, and is designed to aid executives and management within sales, business development, and marketing organizations in making important strategic and product development decisions. Taken together, the qualitative analysis of the covered market and application segments, and the historical and forecast data will enable companies and individuals to better understand the status of—and to anticipate market and technology trends in—the constantly evolving IC market.

1.2 Report Organization

This report is organized into seven chapters:

- Chapter 1 – Introduction - Outlines the scope and organization of the report. It also includes an extensive glossary of semiconductor and packaging terms and acronyms.
- Chapter 2 – Executive Summary - Provides an overview of the markets covered in this report and highlights of the top-level market segments.
- Chapter 3 – Global Electronics Market Trends and Forecasts - Examines the world economy and government and technology forces driving the semiconductor industry. Provides a systems-level view of the electronics sector, including forecasts of assembly value for eight major market sectors. Also provides analysis of ICs used in selected electronics products. Major sections consist of:
    - Recent Global Electronics Market Trends
    - Global Electronics Market
    - Electronics Industry Summary Forecast
- Chapter 4 – Overview of IC Devices and Packaging Markets - Gives a high-level view of the market for integrated circuits and the various packaging types used with ICs. Defines the market segments and forecasts IC device types as well as fourteen categories of packaging form defined by NVR. Major sections consist of:
    - Semiconductor Sector Industry Trends
    - Worldwide IC Devices Market

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    - Worldwide IC Packaging Market
- Chapter 5 – IC Applications Analysis - Drawing on the market analysis provided in Chapter 4, defines and forecasts five major application segments for both IC devices and IC packaging market segments. Forecasts of unit shipments, revenues, and segment share of market are provided for each market segment. Also provides a section analyzing flip chip packaging for application segments. Major sections consist of:
    - Semiconductor Devices Applications Trends
    - IC Device Applications Market Analysis
    - IC Packaging Applications Market Analysis
    - Flip Chip Interconnection Applications Trends
- Chapter 6 – OSAT Market and Strategy Analysis - Presents an overview of the outsourced semiconductor assembly and test market—a subset of the total IC packaging market—as well as forecasts and market trends. Major sections consist of:
    - Outsourcing in the Semiconductor Market
    - Semiconductor Industry Consolidation
    - OSAT Market Forecasts
    - Success Strategies for OSATs
    - OSAT Market Leaders
- Chapter 7 – OSAT Company Profiles - Provides company overview, IC packaging product descriptions, and principal manufacturing facilities of 39 companies that compete in the OSAT market.

1.3 Glossary of Packaging Terms

Listed below are terms and acronyms used in the semiconductor industry, with particular emphasis on packaging terminology. Terms contain definitions, while acronyms are provided with the full term for which it applies and when appropriate a longer definition.

ACA – Anisotropic Conductive Adhesive

ACF – Anisotropic Conductive Film

ACP – Anisotropic Conductive Paste

Area Array – Arrangement of electrodes (bond pads or solder balls) in an area covering the entire face of the package or substrate rather than only the periphery

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ASIC – Application-Specific Integrated Circuit. Integrated circuits designed for or by a specific customer for a specific purpose.

ASP – Average Selling Price

ASSP – Application-Specific Standard Product. An IC designed to implement a specific function or application, but not designed as a standard, or off-the-shelf, product.

ATE – Automated Test Equipment

Bare Die – Unencapsulated silicon in singulated form

BGA – Ball Grid Array. Die mounted on a small printed circuit board (like FR-4) with solder-bumped "leads" on the bottom to create a microcarrier package capable of being surface-mounted to ordinary printed circuit boards.

BIST – Built-In Self-Test. A design technique that enables an IC to test itself.

BOC – Board on Chip. Package designs with the substrate bonded to the circuit side of the die, and wire bonds connected between the conductors of the substrate and the bond pads on a die.

C4 – Controlled Collapse Chip Connection. Another term for flip chip. Originally developed by IBM.

CAGR – Compound Annual Growth Rate

Capacitance – The property of a system of conductors and dielectrics that permits storage of electricity when potential differences exist among the conductors. The capacitance value is always positive and is expressed as the ratio of quantity of electricity to a potential difference.

Capacitor – A device whose function is to introduce capacitance into the circuit. It is made of two insulating surfaces separated by an insulating material or dielectric such as air, mica, glass, plastic film, or oil. It stores electrical energy, blocks the flow of direct current, and allows the flow of alternating current. A capacitor is also called a condenser.

CBGA – Ceramic Ball Grid Array

CC – Chip Carrier

CCC – Ceramic Chip Carrier

CCD – Charge-Coupled Device

CCGA – Ceramic Column Grid Array

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CDIP or CERDIP – Ceramic Dual In-line Package. This is a hermetic package consisting of two pieces of dry-pressed ceramic surrounding a "dip formed" leadframe.

CLCC – Ceramic Leadless Chip Carrier

CLGA – Ceramic Land Grid Array

CMOS – Complementary Metal-Oxide Semiconductor

COB – Chip On Board. A direct chip attachment method to mount an unencapsulated die to a printed circuit board (or MCM-L). Wire bonding is used to connect the signals to the circuit board, and an epoxy encapsulation over the die and wires provides environmental protection.

COF – Chip On Film or Chip on Flex

COG – Chip On Glass. A low-cost solution for LCD driver or controller ICs. The chip is attached directly onto a glass panel with conductive adhesive paste.

CPGA – Ceramic Pin Grid Array

CPLD – Complex Programmable Logic Device

CQFP – Ceramic Quad Flat Pack

CSIC – Customer-Specific Integrated Circuit. Term coined by Motorola. Similar to ASIC. (Compare with ASSP.)

CSP – Chip-Scale Package. A high-density package that approximates the size of the chip itself. These packages can be classified as FBGA, DSBGA, QFN, DFN, and WLP.

CTE – Coefficient of Thermal Expansion

CVD – Chemical Vapor Deposition

DCA – Direct Chip Attach. Encompasses all forms of bare die attachment, including COB, FCOB, and TAB.

DFN – Dual Flat pack, No lead. A leadframe chip-scale package.

DFT – Design for Test

DPAK – Discrete packaging

Die Attach – The process of attaching the die to the leadframe by using a specified type of epoxy/adhesive

Die Stack – A form of stacked package in which two or more die are stacked up within a single package

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DIP – Dual In-line Package

DSBGA – "Die-Size" Ball Grid Array. A chip-scale package that has polyimide or other film as an interposer or substrate, and very closely follows the outline of the actual die.

DUT – Device Under Test

EBGA – Enhanced Ball Grid Array

ELK – Extra low-K (dielectric)

EM – Electromigration

Fabless Manufacturing (Fabless Semiconductor Company) – Refers to a company that designs semiconductors, but does not have in-house manufacturing facilities. Such companies outsource wafer production to a semiconductor Foundry. IC packaging and testing services are generally outsourced to an OSAT. Compare to IDM, or Integrated Device Manufacturer.

FBGA – Fine-pitch Ball Grid Array. A chip-scale package that is slightly larger than the DSBGA, with a firmer substrate.

FCBGA – Flip Chip Ball Grid Array

FCIP – Flip Chip In Package

FCOB – Flip Chip On Board. A method of bare die attachment face down on an FR-4 PCB.

FCOC – Flip Chip On Ceramic. A method of bare die attachment face down on a ceramic surface.

FCOG – Flip Chip On Glass

Flip Chip – A method for interconnecting semiconductor devices to external circuitry. The device is flipped—inverted so that the leads are face down—and connected to a package, substrate, or board. The chip typically has bumps (on the bond pads) in a peripheral or array design.

FOWLP – Fan-Out Wafer-Level Packaging

Foundry (also Semiconductor Fabrication Foundry or Fab) – A contract manufacturer that builds semiconductors or assembles ICs designed by other companies, typically by fabless semiconductor companies. See also Fabless Manufacturing.

FPGA – Field-Programmable Gate Array. Devices that use a grid of logic gates on which the data, once programmed, does not change. They differ from ordinary gate arrays by being "field-programmable" by the user.

FQFP – Fine-pitch Quad Flat Pack

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GaAs – Gallium Arsenide. An alloy of gallium and arsenic that is used as the base material for compound (multi-element) semiconductors. It is several times faster than silicon and is used in high-frequency, high-speed, low-power applications such as cell phones. It is particularly effective for manufacturing the RF front ends of cellular/PCS handsets, the part that broadcasts and detects the signal.

HAST – Highly Accelerated Stress Test

HCTE – High Coefficient of Thermal Expansion

HDIS – High-Density Interconnect Structure

Heat Sink – A device, usually metal, utilized to extract and dissipate heat

Heat Slug – Usually denotes a "drop-in" metal device that is used with conventional leadframes having die attach paddles. The heat slug is typically not attached with adhesive or fixed to the leadframe.

I/O – Input/Output

IC – Integrated Circuit

IDM – Integrated Device Manufacturer

ICA – Isotropic Conductive Adhesive

ILCC – Integrated Lead Chip Carrier

IPC – An industry association for printed circuit board and electronics manufacturing service companies. Originally founded in 1957 as the Institute for Printed Circuits, later changed to Institute for Interconnecting and Packaging Electronic Circuits, and from that to simply IPC, in 1999. Its identifying slogan is "Association Connecting Electronics Industries."

IVH – Inner Via Hole

Integrated Device Manufacturer – A company that designs, manufactures, and sells ICs. Compare to Fabless Manufacturing.

JEDEC Solid State Technology Association – Formerly known as the Joint Electron Device Engineering Council, and still commonly referred to by the acronym JEDEC. A major open standards organization for the microelectronics industry. Established in 1958, and today has more than 300 member companies.

JEITA – Japan Electronics and Information Technology Industries Association. Formed in 2000 by the merger of the Electronic Industries Association of Japan (EIAJ) and Japan Electronic Industries Development Association (JEIDA).

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KGD – Known Good Die. A tested bare chip that has the same level of performance, reliability, and quality as its packaged version. Typically used in multichip modules.

Leadframe (also Lead Frame) – The metal structure inside a chip package that carries the electrical signal from the die to the external connectors. Typically uses wire bonding to connect the die pads to the I/O leads. Most commonly used with quad flat pack packages, quad flat pack no-lead packages, and dual in-line packages.

LGA – Land Grid Array

LLCC – Leadless Chip Carrier (ceramic)

LOC – Lead On Chip

LQFP – Low-profile Quad Flat Pack

LTCC – Low-Temperature Cofired Ceramic

MAP – Molded Array Package

mBGA – Mini Ball Grid Array

µBGA (also MBGA) – Micro Ball Grid Array. Developed by Tessera, Inc. µBGA is a registered trademark of Tessera, Inc.

MCM-C/D – Multichip module with thin film deposited on ceramic substrate

MCM-C – Multichip module with cofired ceramic substrate

MCM-D – Multichip module that utilizes a silicon substrate with deposited thin films

MCM-L/D – Multichip module with thin film deposited on laminate

MCM-L – Multichip Module–Laminate. A low-cost MCM that uses printed circuit board–like organic materials (e.g., FR-4) as a substrate.

MCM-LO – Multichip Module–Laminate/thin film Overlay

MCM-PBGA – Multichip Module–Plastic Ball Grid Array

MCM – Multichip Module. A functional collection of stand-alone blocks of silicon in either "bare" die form or some other surface-mountable micro packaging, mounted on various substrates from printed circuit boards to ceramic and thin film structures and delivered as a highly integrated module. First used in the 1970s and a precursor to modern system-in-packages.

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MCP – Multichip Packaging. Any package containing two or more ICs. Differs from MCM in that this is not a stand-alone system of any kind, and is basically a collection of die within a single package.

MEMS – Micro**e**lectro**m**echanical System

µPGA or **mPGA** – microPGA

Modulus – *see* Young's Modulus

MOEMS – Micro-Optoelectromechanical System

MOS – Metal-Oxide Semiconductor

MQFP – Metric Quad Flat Pack

MRQFN – Multi-row Quad Flat Pack No Lead

NCP – Nonconductive Paste

Nonvolatile Memory – Semiconductor memory that continues to retain data even when there is no power going to the chip. Read-only memory (ROM) and flash memory are nonvolatile. Compare with Volatile Memory.

OSAT – Outsourced Semiconductor Assembly and Test. Provides back-end semiconductor manufacturing services to package ICs and perform final test of the completed package. See also Fabless Semiconductor Company.

PBGA – Plastic Ball Grid Array

PCB – Printed Circuit Board

PDIP – Plastic Dual In-line Package

PGA – Pin Grid Array

PI – Polyimide

PiP – Package-in-Package. A method of stacked packaging in which multiple dies are vertically stacked within a single package form, such as an FBGA.

PLCC – Plastic Leaded Chip Carrier

PoP – Package-on-Package. A method of stacked packaging in which individual, fully tested packages are vertically stacked on top of each other.

PPGA – Plastic Pin Grid Array

PQFP – Plastic Quad Flat Pack

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PTH – Plated Through-Hole

PTFE – Polytetrafluoroethylene

PWB – Printed Wiring Board (also known as Printed Circuit Board)

QFN – Quad Flat pack, No lead

QFP – Quad Flat Pack. A surface-mount package with leads on all four sides. The package body can be ceramic, metal, or plastic.

RoHS – Restriction of Hazardous Substances. Also known as Directive 2002/95/EC, this directive originated in the European Union and restricts the use of six hazardous materials commonly found in electrical and electronic products. The materials are lead, mercury, cadmium, hexavalent chromium (CrVI), polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE).

SDBGA – Stacked-Die Ball Grid Array

SESUB – Semiconductor Embedded in SUBstrate

Si – Silicon

SiB – System-in-Board

SiP – System-in-Package. Can be one or more semiconductor die and passives (resistors and/or capacitors), or two or more chips that form a system or functional block.

SIP – (All caps) Single In-line Package

SLIC – Subscriber Line IC (for telecommunications applications)

SMT – Surface-Mount Technology

SO – Small Outline

SoC – System-on-Chip. A single large-scale chip incorporating multiple technologies into a complete system.

SoP – System-on-Package. Similar to a SiP, in that multiple die and passives are combined in a single package. When a distinction is made, a SoP is considered using a substrate built up using organic buildup technology, while a SiP can use a laminated substrate.

Socket – A slot, often on a PCB or motherboard, that provides a mechanical and electrical connection for a component to the board. The device is usually held in place by retention clips or a similar mechanism, which makes it possible to replace components without soldering.

SOIC – Small Outline Integrated Circuit

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SOJ – Small Outline J lead

SON – Small Outline No lead (now referred to as QFN)

SOP – Small Outline Package (also known as SOIC)

SOT – Small Outline Transistor

SSOP – Shrink Small Outline Package

Stacked Package – IC packages that are stacked vertically. Can be a variety of configurations, including stacking bare die within a single package (die stack), or multiple individual packages stacked on top of each other (package stack or package-on-package). The interposer can be a substrate or leadframe.

Substrate – A semiconductor medium, such as silicon or gallium arsenide, that provides the foundation for the construction of components of an IC. The substrate is formed in wafers on which the electronic components are etched or fabricated and bumps provide the electical connection to the system board.

Surface Mount – A term used to describe a package whose leads or terminals are attached to the surface of the PC board with solder paste

TAB – Tape Automated Bonding; also called Tape Carrier Package. Uses a flexible carrier tape, typically copper/polyimide, to connect the chip to the package, substrate, or board.

TCP – Tape Carrier Package

THB – Temperature/Humidity Bias

Through-hole – A term used to describe a package whose leads are attached through drilled holes in the PC board

Through-silicon via (TSV) – A via that extends through silicon, used either within a lower die in a die stack (3D) or within a silicon interposer between two die (2.5D), and that provides the electrical connection between the die in the stack and the substrate below

THT – Through-Hole Technology

TO – Transistor Outline

TQFP – Thin Quad Flat Pack

Transistor – A device used to amplify a signal or open and close a circuit. The transistor contains a semiconductor material that can change its electrical state when pulsed.

TSOP – Thin Small Outline Package

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TSSOP – Thin Shrink Small Outline Package

TSV – Through-Silicon Via. A technique of interconnecting die with vias (holes) made through the silicon.

TVSOP – Thin Very Small Outline Package

UBM – Under-Bump Metallization

UFBGA – Ultra-thin profile Fine-pitch Ball Grid Array

VFBGA – Very thin Fine-pitch Ball Grid Array

VIA – Vertical Interconnect Access. A vertical electrical connection used in advanced packaging techniques to create 3D packages.

Volatile Memory – Memory semiconductors that cannot hold data information when there is no power going to the device. DRAM is the best example of this type of memory. Compare with Nonvolatile Memory.

Wafer Bumping – Process of applying bumps of solder or gold to the die pads so they can be utilized for flip chip or TAB interconnection. Bumps provide the electrical connection to the PCB.

WFBGA – Very Very thin profile Fine-pitch Ball Grid Array

Wire Bonding – The primary method of electrically connecting a die to a package

WLP – Wafer-Level Package

Young's Modulus – The stress of a material divided by its strain. That is, how much the material yields for each pound of load put on it. It is a measure of tensile elasticity and strength. Loosely, the modulus is defined as the force needed to elongate material.

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